

ABSTRACT OF THE DISCLOSURE

A multi-valued logic emulation system reads a specifying value for specifying with which value, logic emulation is performed, and represents the logic value by a plurality of physical signal lines equal to (\log_2 a raised integer of the specifying value). Then, the system performs multi-value supporting synthesis and automatic place/automatic route processing, and maps resulting information to a programmable gate array, thereby making it possible to execute multi-valued logic emulation.

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